CLAIMS

What is claimed is:

1. A finite state automata building block comprising:

a plurality of node elements that store a current state of a finite state automata evaluation;

a plurality of programmable interconnections that fully connect the plurality of node elements;

a symbol evaluation unit having a corresponding symbol for each of the node elements, the symbol evaluation unit evaluating an input to provide a symbol match determination;

a state transition evaluation logic that transitions the node elements from one set of states to another set of states upon receiving a determination of a symbol match and enabled interconnection;

a node element initialization mechanism to initialize the node elements to a specified value;

an evaluation termination mechanisms to determine if the node elements have reached a specified evaluation termination state; and

a stitching mechanism that activates a set of programmed state transitions of one or more target finite state automata building blocks upon detection of a specific state of the node elements.

2. The finite state automata building block of claim 1 wherein the stitching mechanism includes one or more registers to specify the specific state.

3. The finite state automata building block of claim 2 wherein the stitching mechanism includes one or more registers to identify the one or more target finite state automata building blocks.

4. The finite state automata building block of claim 1 wherein activating a set of programmed state transitions comprises:

combining the set of programmed state transitions with a current state of a finite state automata evaluation of the target.

5. The finite state automata building block of claim 1 wherein the finite state automata building block is connected to one or more target finite state automata building blocks via a set of interconnections.

6. A finite state automata building block comprising:

a plurality of node elements that store a current state of a finite state automata evaluation;

a plurality of programmable interconnections that fully connect the plurality of node elements;

a symbol evaluation unit having a corresponding symbol for each of the node elements, the symbol evaluation unit evaluating an input to provide a symbol match determination;

a state transition evaluation logic that transitions the node elements from one set of states to another set of states upon receiving a determination of a symbol match and enabled interconnection;

a node element initialization mechanism to initialize the node elements to a specified value; and

two or more evaluation termination mechanisms each of which determines if a corresponding set of the node elements has reached a corresponding specified evaluation termination state.

7. The finite state automata building block of claim 6 wherein each of the two or more evaluation termination mechanisms includes a register containing the corresponding specified evaluation termination state.

8. The finite state automata building block of claim 6 wherein each of the two or more evaluation termination mechanisms includes a register to indicate that the corresponding specified evaluation termination state has been reached.

9. A device comprising:

one or more finite state automata building blocks; and

a finite state automata building block controller to communicate information between the one or more finite state automata building blocks and a memory device.

10. The device of claim 9 wherein the information is state information of the one or more finite state automata building blocks.

11. The device of claim 10 wherein the state information is read from the one or more finite state automata building blocks by the finite state automata building block controller at a specified point of an input data stream.

12. The device of claim 11 wherein the specified point is an interruption point of the input data stream.

13. The device of claim 12 wherein the state information is written to the one or more finite state automata building blocks by the finite state automata building block controller upon continuation of processing of the interrupted input data stream.

14. The device of claim 10 wherein the state information comprises a value of a set of node elements of the one or more finite state automata building blocks.

15. The device of claim 14 wherein the state information further comprises a counter value.

16. The device of claim 9 wherein the information is rule information for defining a regular expression implemented on the one or more finite state automata building blocks.

17. The device of claim 16 wherein the finite state automata building block controller dynamically reprograms the one or more finite state automata building blocks using the rule information.

18. The device of claim 17 wherein the reprogramming is in response to detecting that the finite state automata building blocks are not programmed to evaluate a specified regular expression.

19. The device of claim 10 wherein the one or more finite state automata building blocks, the finite state automata building blockcontroller, and the memory device are implemented on a same integrated circuit chip.

20. The device of claim 10 wherein the one or more finite state automata building blocks comprise a plurality of finite state automata building blocks organized in fully interconnected groups.

21. The device of claim 10 the one or more finite state automata building blocks comprise a plurality of finite state automata building blocks organized partitioned into groups, the size of each group based upon a number of regular expressions to be evaluated, each group receiving an independent data stream such that the independent data streams are processed concurrently.

22. A finite state automata building block comprising:

a plurality of node elements that store a current state of a finite state automata evaluation;

a plurality of programmable interconnections that fully connect the plurality of node elements;

a symbol evaluation unit having a corresponding symbol for each of the node elements, the symbol evaluation unit evaluating an input to provide a symbol match determination;

a state transition evaluation logic that transitions the node elements from one set of states to another set of states upon receiving a determination of a symbol match, enabled interconnection, and a counter that counts the occurrence of a specified set of states having reached a specified counter value;

a node element initialization mechanism to initialize the node elements to a specified value; and

an evaluation termination mechanisms to determine if the node elements have reached a specified evaluation termination state.

23. The finite state automata building block of claim 22 wherein the occurrence of the specified set of states is a part of a regular expression definition.

24. The finite state automata building block of claim 23 wherein the specified set of states is contained in a state specification register.

25. The finite state automata building block of claim 23 wherein the specified counter value is contained in a counter value register.